THREE-DIMENSIONAL MMIC ARCHITECTURE USING LOW THERMAL IMPEDANCE TECHNOLOGY

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ABSTRACT

A novel architecture for monolithic microwave integrated circuits (MMICs) simultaneously provides significant reduction in die area and extremely efficient heat transfer, as evidenced by 2 x 2 mm^2 MMICs which deliver up to 40 W CW at 1.8 GHz.

INTRODUCTION

Monolithically-integrated impedance matching networks (hereinafter referred to simply as "networks") allow fabrication of microwave and millimeter-wave circuits with a degree of reproducibility which would otherwise be unobtainable. However, these networks do have certain drawbacks. The first and most obvious drawback is that the passive components comprising these networks usually occupy most of the expensive semiconductor die area. A second (and perhaps less obvious) drawback is that the planar nature of the networks generally requires that the heat-dissipating transistors be closely spaced in linear arrays. Such an arrangement is undesirable from a thermal perspective, since each transistor contributes significant heating to neighboring devices.

We report a revolutionary MMIC architecture which addresses both of these drawbacks by placing passive components in the same "footprint" on opposite sides of the die (for up to 50% die size reduction) while simultaneously spacing the transistors evenly across the die in a two-dimensional array. This arrangement approaches the ideal thermal design by minimizing thermal coupling between adjacent devices, allowing the entire die area to transfer heat to the heatsink. Such an arrangement is not used in conventional MMICs because of the need to maintain proper signal phase for the input and output of every transistor in the two-dimensional array -- a feat which is not practical in a single plane. Therefore, in order to maintain as much symmetry as possible for the matching networks, conventional "single-plane" MMICs are generally designed with the transistors in a linear array.

However, Low Thermal Impedance (LTI) MMICs contain not one, but two planes: transistors, thin-film resistors, capacitors, and microstrip transmission lines are fabricated on the side of the chip which is against the heat sink ("active side"), and additional capacitors and microstrip lines are fabricated on the opposite side of the chip ("passive side") [1]. These two planes are clearly not independent, since they are on opposite sides of a single GaAs chip. Nevertheless, we found the prospect of realizing a near-optimum thermal layout while greatly reducing the area required for passive components to be sufficiently attractive to warrant further investigation -- particularly since no process development would be required.

LTI also was attractive as a technological foundation for the present work because of the extreme performance enhancement it provides. LTI HBTs have achieved not only record power-efficiency performance (20 W / 80% PAE at 1.3 GHz, and 20 W / 64% PAE at 2 GHz, both at 28 V), but also record power density as well [2]. At >30 W per square millime-

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ter of die area, discrete LTI-HBTs far exceed the power density of any other III-V microwave technology, and deliver almost twice the highest CW power density reported for any SiC device to date at microwave frequencies in terms of Watts per unit area of die [3].

We therefore investigated and addressed various issues associated with design of microwave circuits using both sides of a nonconductive die. We refer to the resulting overall approach, which has been implemented entirely within the existing LTI process technology, as Three-Dimensional MMIC Architecture, or 3DMA.

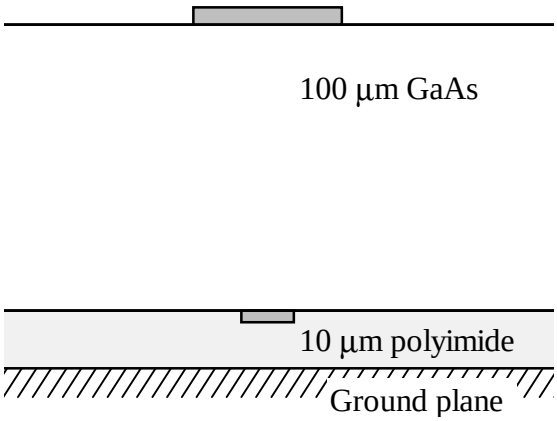

Figure 1. Cross-sectional diagram of 50 Ω microstrip lines on opposite sides of GaAs chip. Signal propagation is perpendicular to the plane of the illustration.

3DMA DESIGN ISSUES

Several issues had to be addressed before the 3DMA concept could be reduced to practice. These issues included isolation between components on opposite sides of the GaAs chip; the properties of the transmission lines on the active side of the chip; and the properties of the transmission lines on the passive side of the chip.

The first issue addressed was that of isolation between components on opposite sides of the GaAs chip. We characterized isolation properties of two parallel 50 Ω microstrip lines on the active and passive sides of 100-μm thick GaAs (as shown in Figure 1) using the electromagnetic simulater from SONNET™. The dimensions and properties for the conductive and insulating layers were taken from the LTI process: the passive-side microstrip line used 100 μm of GaAs plus 10 μm of polyimide as the dielectric, while the active-side line was between the GaAs and polyimide layers. The length along which the two lines overlapped was held constant at 200 μm. This line length was chosen because it exceeds any foreseeable overlap which might be required for a 3DMA amplifier design. Even in this worst-case analysis, the predicted coupling was less than -30 dB for frequencies up to 15 GHz. With such a high degree of isolation, coupling may be neglected for many cases of interest, and standard circuit design techniques may be applied.

The second issue concerned the properties of the transmission lines on the active side of the chip. In order to be easily incorporated into the MMIC design process, these lines must have predictable properties. As shown in Figure 1, these lines operate in microstrip mode with 10 μm of polyimide dielectric separating them from the ground plane. However, some of the electric field “spills over” into the overlying GaAs substrate, so that the effective dielectric constant of these embedded transmission lines is dependent on the ratio of the line width to the dielectric thickness. We calculated the effective dielectric constant as a function of the width-to-height ratio using electromagnetic simulations. After fitting an equation to the resulting curve, we added a user-defined element to the circuit design software so that active-side transmission line elements could be designed and optimized in the same way as conventional microstrip lines.

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The final issue to be addressed concerned the properties of the passive-side transmission lines. Over most of the area of the chip, these lines are identical to conventional microstrip lines, with 100 μm of GaAs as the dielectric material. However, where a passive-side microstrip crosses an active-side transmission line (or other non-grounded circuit element on the active side of the chip), there is a transition between dielectric composed of 100 μm of GaAs, and dielectric composed of 100 μm GaAs plus 10 μm of polyimide. Although the GaAs is very thick compared to the polyimide, the lower dielectric constant of the polyimide (roughly 1/3 that of GaAs) could potentially cause such a transition to have a significant impact. Fortunately, electromagnetic simulations confirm that this transition has negligible effect as long as the passive-side microstrip does not traverse the GaAs-polyimide stack for a significant fraction of a wavelength. This condition is easily satisfied for cases of interest for power amplifiers.

3DMA CIRCUIT DEMONSTRATION

With the properties of active- and passive-side microstrip lines established, the design procedure for 3DMA circuits is identical to that for conventional MMICs. As an initial demonstration of the 3DMA concept, we designed a single-stage power amplifier consisting of the simplest two-dimensional array of unit cells: a 2×2 array. The unit cell consists of twenty emitter fingers, each 4×100 μm^2, with 40 μm pitch. Figures 2 and 3 show the active and passive sides of the 3DMA die, which is 2×2 mm^2. The output matching network was implemented entirely on the passive side of the chip; components for the input network were placed on both sides of the chip to minimize die size. Note that the network on the passive side overlaps not only active-side microstrip lines, but also capacitors, resistors, and even transistors on the active side.

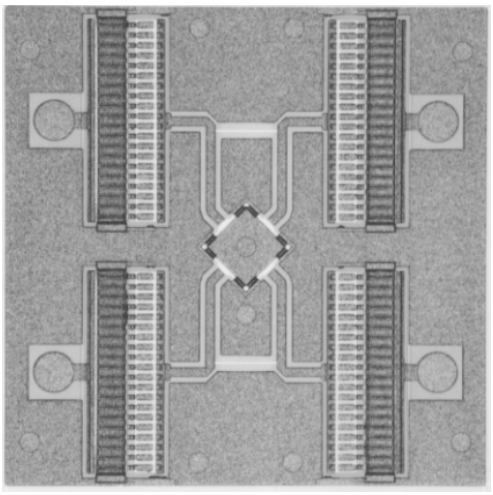

Figure 2. Active side of 3DMA amplifier

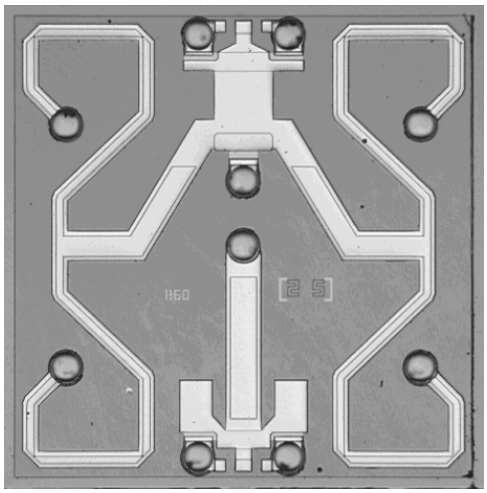

Figure 3. Passive side of 3DMA amplifier

While the design procedure was identical to that for a conventional MMIC, the design itself involved quite a bit of approximation since the input and output impedances of the unit cells were unknown at the time of the design. We therefore based the amplifier design on projected input and output impedances derived from scaling of X-band HBT unit cells, which are much smaller and use smaller-valued bypass capacitors in the thermal ballast because of the higher operating frequency [4]. The epi structure for the demonstration was similar to that

reported in [2], except that the collector layer was 1 μm thick with a doping concentration of 2 $\times 10^{16}$ cm^{-3} and breakdown voltage of 28 V.

The 3DMA amplifier die was attached to a gold-plated copper fixture using solder. The matching networks in the amplifier were found to perform surprisingly well considering the degree of uncertainty involved in the estimated input and output impedances of the unit cell; however, some external tuning was required to achieve best performance under large-signal conditions. A fixture loss of 0.1 dB was assumed on the output; no other tuner or fixture losses were deembedded for the results presented in this paper, and all testing was performed under CW operation at room temperature baseplate at 1.8 GHz.

The amplifier achieved peak power-added efficiency of 51% at an output power of 31.6 W CW (45 dBm) with 8.6 dB associated gain; collector bias was 10.7 V, with collector current of 4.91 A. Maximum output power of 40 W CW was obtained at V_{CE} = 12 V, I_C = 6.74 A, with 9.5 dB associated gain and 43.8% PAE. At this condition, the relatively small (2 × 2 mm^2) die had a continuous power dissipation of 45 W at room temperature baseplate. Each of the four unit cells was therefore dissipating over 11 W of heat, which is higher than the single-cell dissipation capability reported previously [2]. Thus the LTI / 3DMA approach demonstrates very good thermal scaling properties.

DISCUSSION

It is important to note that this first-pass amplifier design was intended only as a demonstration of the 3DMA concept; no particular care was taken to minimize the losses in the matching circuits. However, the same unit cell design, when applied to a high-voltage epi structure, delivered roughly twice as much RF output power as it dissipated as heat in this frequency range [2]. We therefore expect that a more thorough design for low loss, based on measured impedances and using a high-voltage epi structure, will yield significantly higher CW power levels with no increase in die size.

Despite the simultaneous decrease in die size and increase in output power compared to conventional MMICs, these 3DMA circuits retain an extremely attractive feature of LTI technology: they are drop-in replacements for conventional MMICs, using the same packages and chip-and-wire techniques. No custom packages, exotic substrates, flip-chip alignment, solder bumps, coplanar circuit techniques, or other trappings of flip-chip technologies are required. Moreover, the LTI process is relatively well-established: DC-probe yields in excess of 80% have been achieved for these 30-40 W amplifiers fabricated in our R&D laboratory.

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